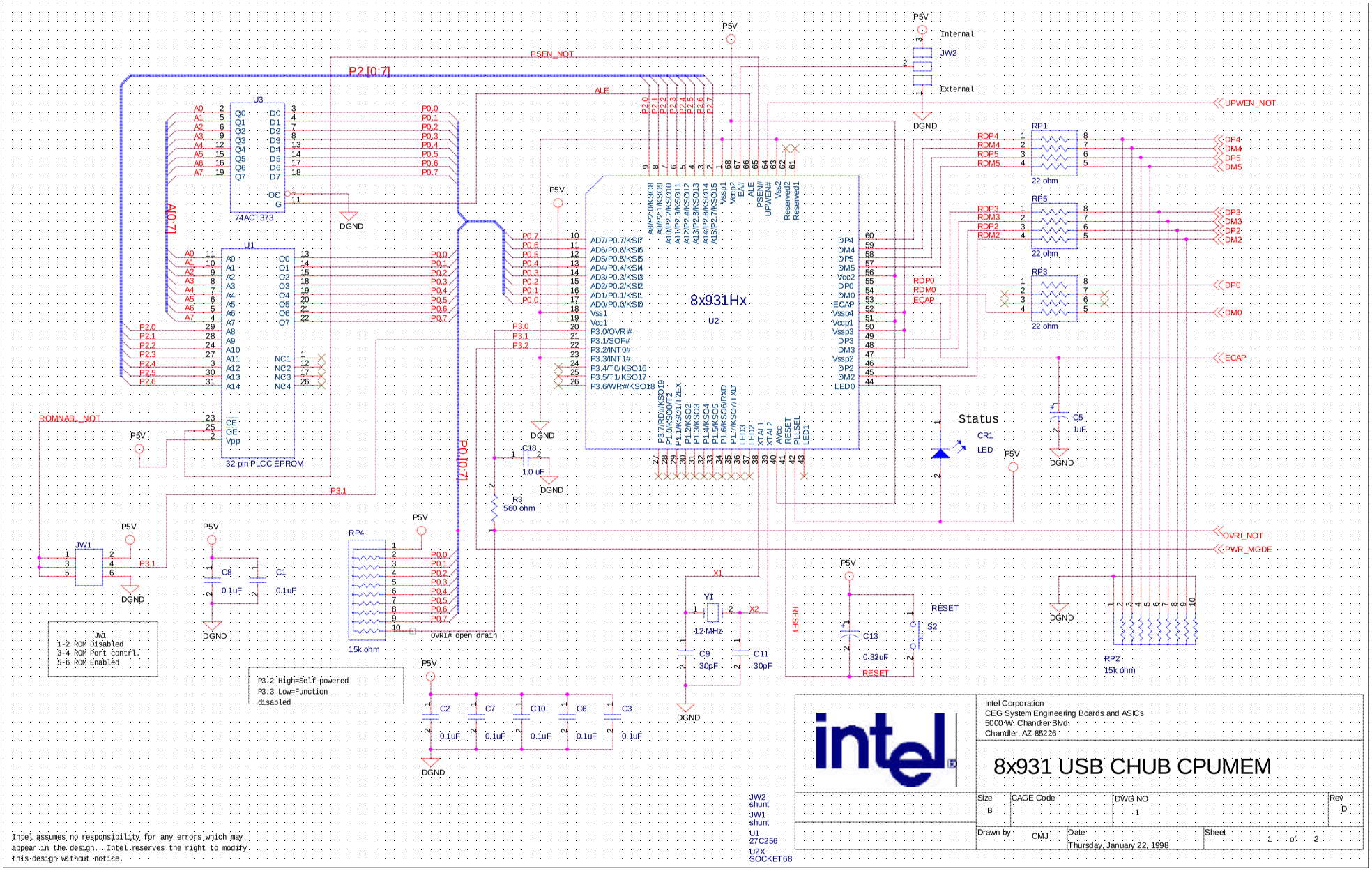
P5V
PSEN_NOT
P2.[0:7]
ALE
Internal
JW2
External
DGND
UPWEN_NOT
U3
74ACT373
A[0:7]
P0.[0:7]
U1
32-pin PLCC EPROM
ROMNABL_NOT
8x931Hx
U2
AD7/P0.7/KSI7
AD6/P0.6/KSI6
AD5/P0.5/KSI5
AD4/P0.4/KSI4
AD3/P0.3/KSI3
AD2/P0.2/KSI2
AD1/P0.1/KSI1
AD0/P0.0/KSI0
Vss1
Vcc1
P3.0/OVR#
P3.1/SOF#
P3.2/INT0#
P3.3/INT1#
P3.4/T0/KSO16
P3.5/T1/KSO17
P3.6/WR#/KSO18
P3.7/RD#/KSO19
P1.0/KSO0/T2
P1.1/KSO1/T2EX
P1.2/KSO2
P1.3/KSO3
P1.4/KSO4
P1.5/KSO5
P1.6/KSO6/RXD
P1.7/KSO7/TXD
LED3
LED2
XTAL1
XTAL2
RESET
PLLSEL
LED1
A8/P2.0/KSO8
A9/P2.1/KSO9
A10/P2.2/KSO10
A11/P2.3/KSO11
A12/P2.4/KSO12
A13/P2.5/KSO13
A14/P2.6/KSO14
A15/P2.7/KSO15
Vssp1
Vccp2
EA#
ALE
PSEN#
UPWEN#
Vcc2
Reserved2
Reserved1
DP4
DM4
DP5
DM5
Vcc2
DP0
DM0
ECAP
Vssp4
Vccp1
Vssp3
DP3
DM3
Vssp2
DP2
DM2
LED0
RP1
22 ohm
RP5
RP3
RDP4
RDM4
RDP5
RDM5
RDP3
RDM3
RDP2
RDM2
RDP0
RDM0
ECAP
DP4
DM4
DP5
DM5
DP3
DM3
DP2
DM2
DP0
DM0
ECAP
Status
CR1
LED
C5
1uF
OVRI_NOT
PWR_MODE
JW1
1-2 ROM Disabled
3-4 ROM Port contrl
5-6 ROM Enabled
C8
0.1uF
C1
0.1uF
RP4
15k ohm
OVRI# open drain
R3
560 ohm
C18
1.0 uF
P3.1
P3.2 High=Self-powered
P3.3 Low=Function disabled
X1
Y1
12 MHz
X2
C9
30pF
C11
30pF
RESET
C13
0.33uF
S2
RP2
15k ohm
C2
C7
C10
C6
C3
0.1uF
JW2 shunt
JW1 shunt
U1: 27C256
U2: SOCKET68
Intel Corporation
CEG System Engineering Boards and ASICs
5000 W. Chandler Blvd.
Chandler, AZ 85226
8x931 USB CHUB CPUMEM
Size B
CAGE Code
DWG NO 1
Rev D
Drawn by CMJ
Date Thursday, January 22, 1998
Sheet 1 of 2
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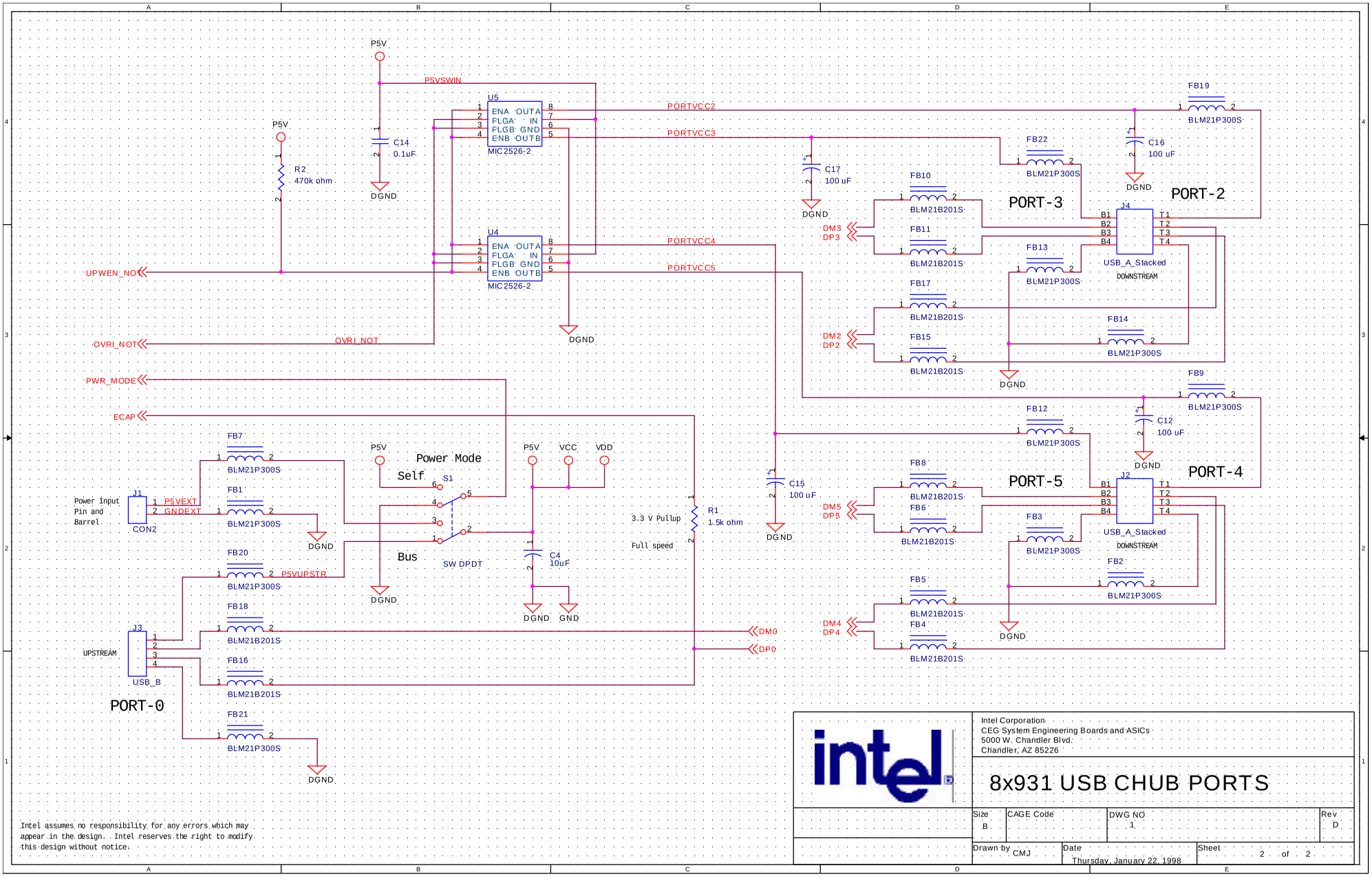

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8x931 USB CHUB PORTS

Size	CAGE Code	DWG NO	Rev
B		1	D

Drawn by	Date	Sheet
CMJ	Thursday, January 22, 1998	2 of 2